

Peak pulse voltage ($T_j=25$; non-repetitive, off-state; FIG.8)	V_{pp}	2.5	kV
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ELECTRICAL CHARACTERISTICS (unless otherwise specified)

Symbol **Test Condition** **Quadrant**

FIG.7: Relative variations of gate trigger current, holding current and latching current versus junction temperature

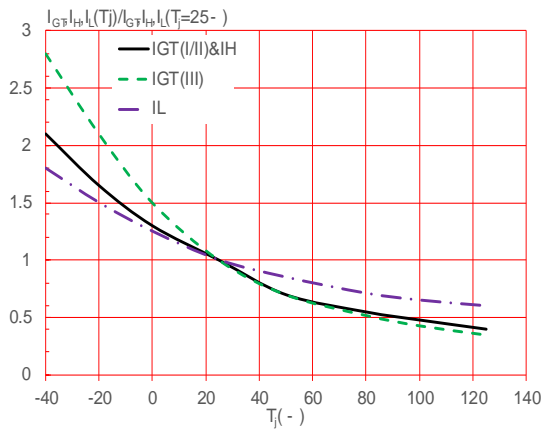
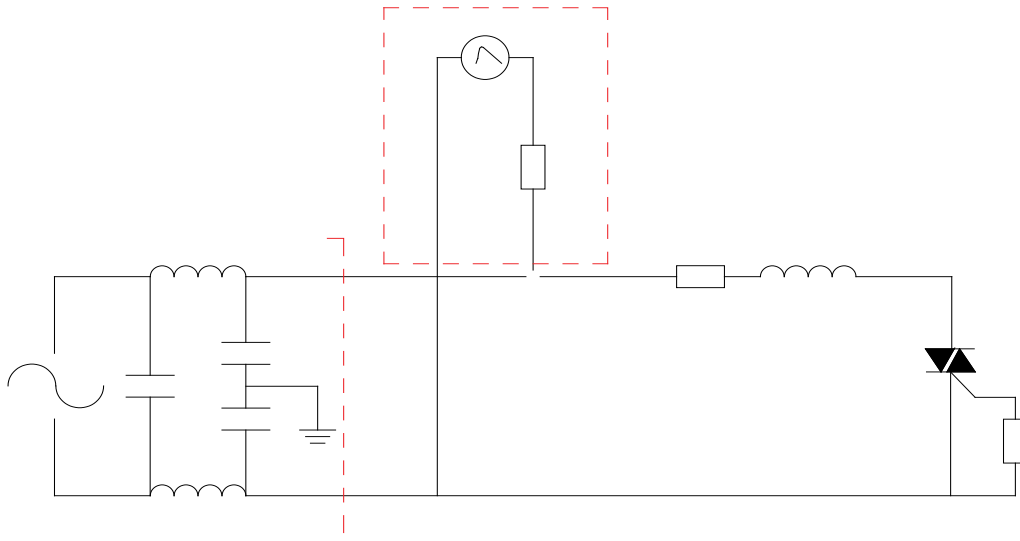


FIG.8: Test circuit for inductive and resistive loads to IEC-61000-4-5 standards



ORDERING INFORMATION

Order cœle	Vdt age V _{DRM} /V _{RRM} (V)	IGT(mA)	Package	Base q y. (œs)	Deli very rœle
		H- I- J			
JST24E-1200CW	1200	35	TO-263	50	Tube
JST24E-1200CW-TR				800	Tape & Reel

Document Revision History

Date	Revision

DELIVERY MODE



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