Peak pulse voltage (T_j=25 ; non-repetitive,off-state;FIG.7)	V_{pp}	2.5	kV

(T_j=25 unless otherwise specified)

Symbol	Test Condition	Quadrant	Value		Unit
I	V_D =12V R_L =33Ω	- -	MAX.	50	
V		- -	MAX.	1	V
V	V_D =V_{DRM} T_j =125 R_L =3.3kΩ	- -	MIN.	0.2	V
I_L	I_G =1.2I_{GT}	-	MAX.	50	mA
				90	
I_H	I_T =100mA		MAX.	50	mA
dV/dt	V_D=800V Gate Open T_j =125		MIN.	500	V/μs
(dI/dt)c	(dV/dt)c=20V/μs, T_j				

t_{on} mA CH0 TdARACTERIS.

J ST 08 C -1200 BW

Year

FIG.1: Maximum power dissipation versus RMS on-state current

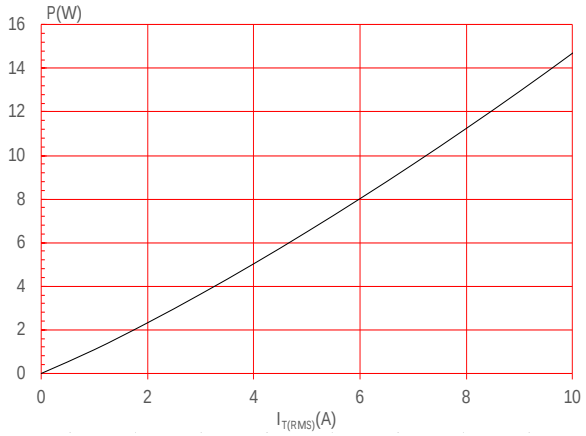


FIG.2: RMS on-state current versus case temperature

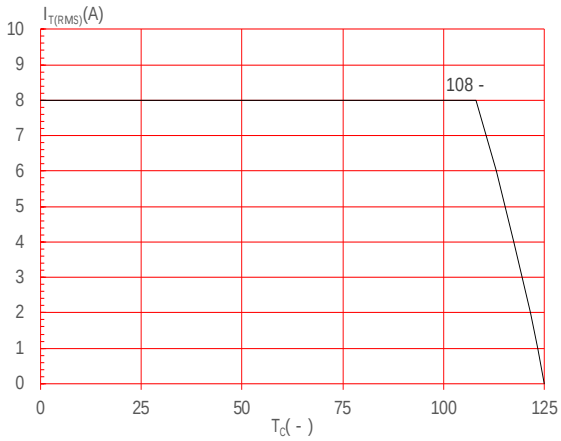


FIG.3: Surge peak on-state current versus number of cycles

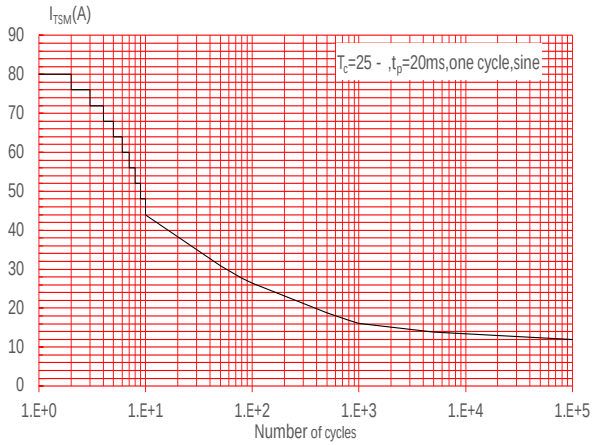


FIG.4: On-state characteristics

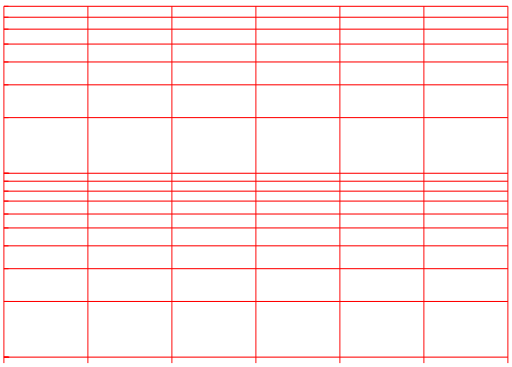
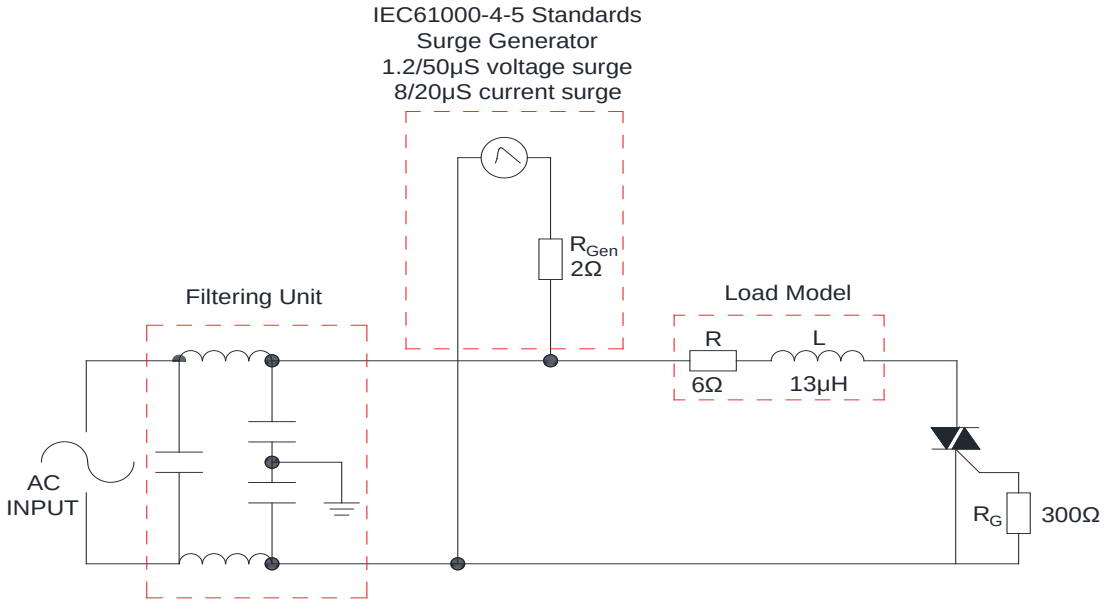


FIG.7 Test circuit for inductive and resistive loads to IEC-61000-4-5 standards



JST08C-1200BW

Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co., Ltd. assumes no responsibility for the consequences of use without consideration for such information nor use beyond it. Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement.

Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information. This document supersedes and replaces all information previously supplied.

is a registered trademark of Jiangsu JieJie Microelectronics Co., Ltd.