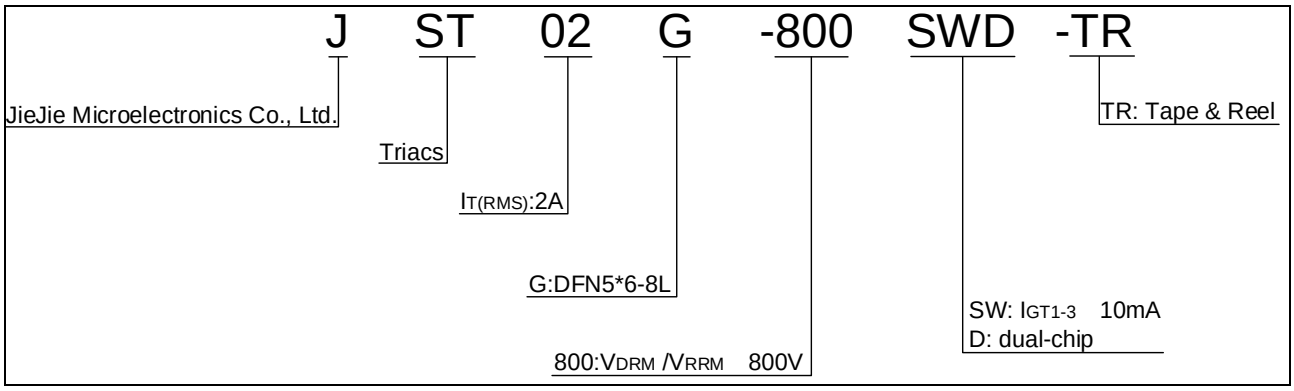
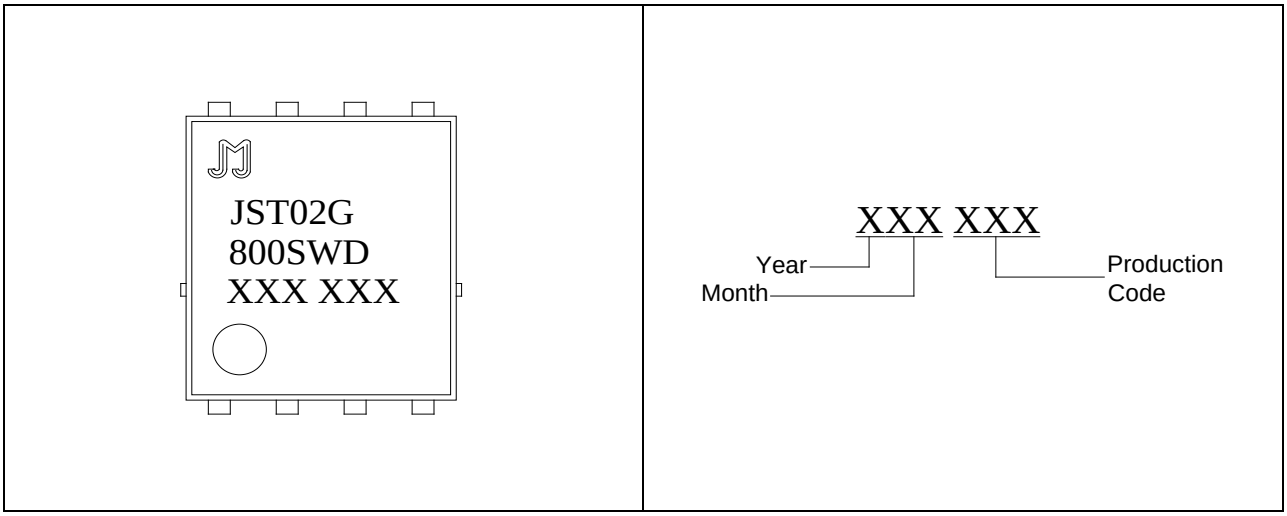
JST02G-800SWD 2A TRIAC

Average gate power dissipation (T_j=125)	$P_{G(AV)}$	0.5	W
Peak gate power	P_{GM}	10	W
Peak pulse voltage (T_j=25 ; non-repetitive,off-state;FIG.8)	V_{pp}	4	kV

(T_j=25 unless otherwise specified)

Symbol	Test Condition	Quadrant	Value		Unit
I_{GT}	V_D =12V R_L =33Ω	- -	MAX.	10	mA
V_{GT}		- -	MAX.	1	V
V_{GD}	V				


J
ST
02
G
-800
SWD
-TR
JieJie Microelectronics Co., Ltd.
Triacs
IT(RMS):2A
G:DFN5*6-8L
800:VDRM /VRRM 800V
SW: IGT1-3 10mA
D: dual-chip
TR: Tape & Reel

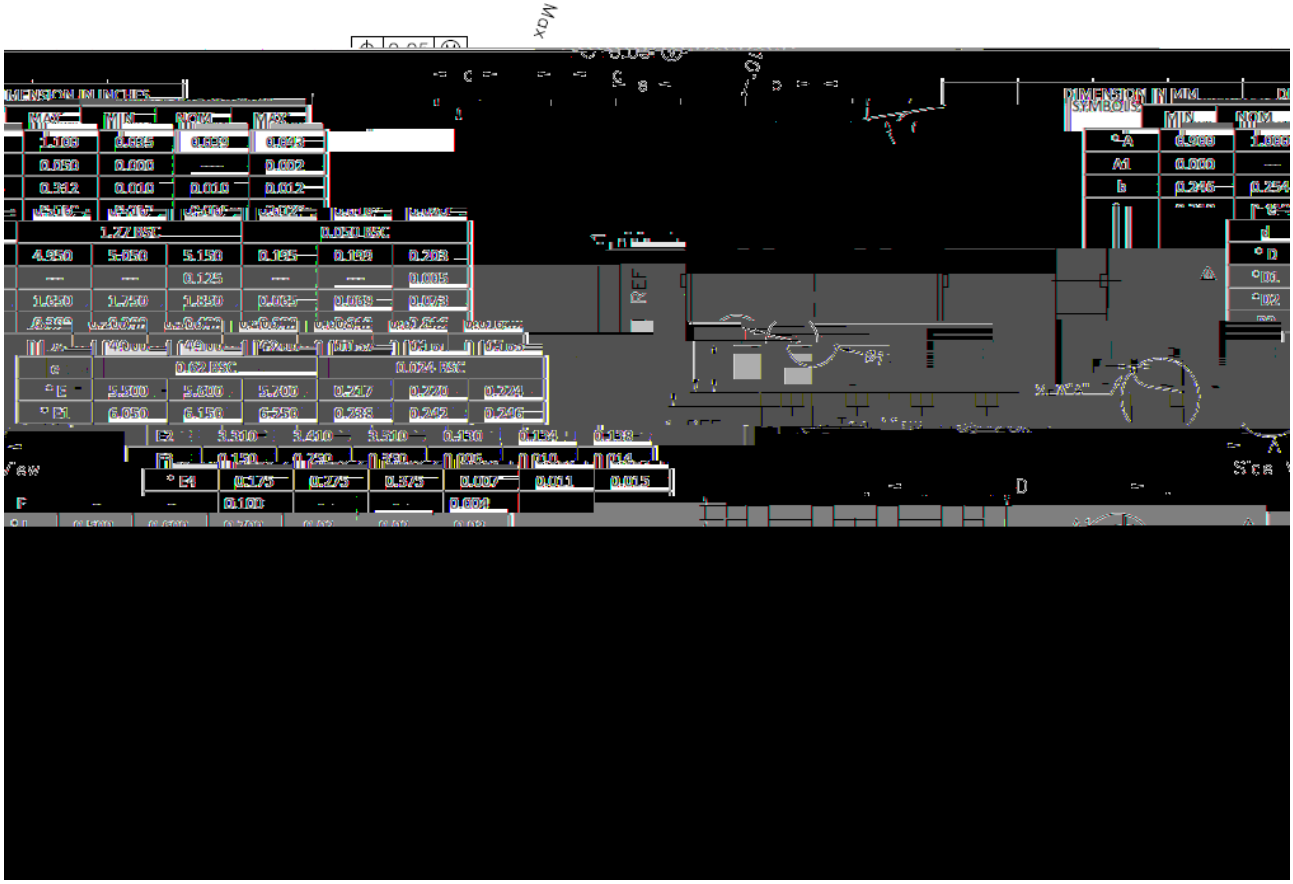

JST02G
800SWD
XXX XXX
XXX XXX
Year
Month
Production
Code

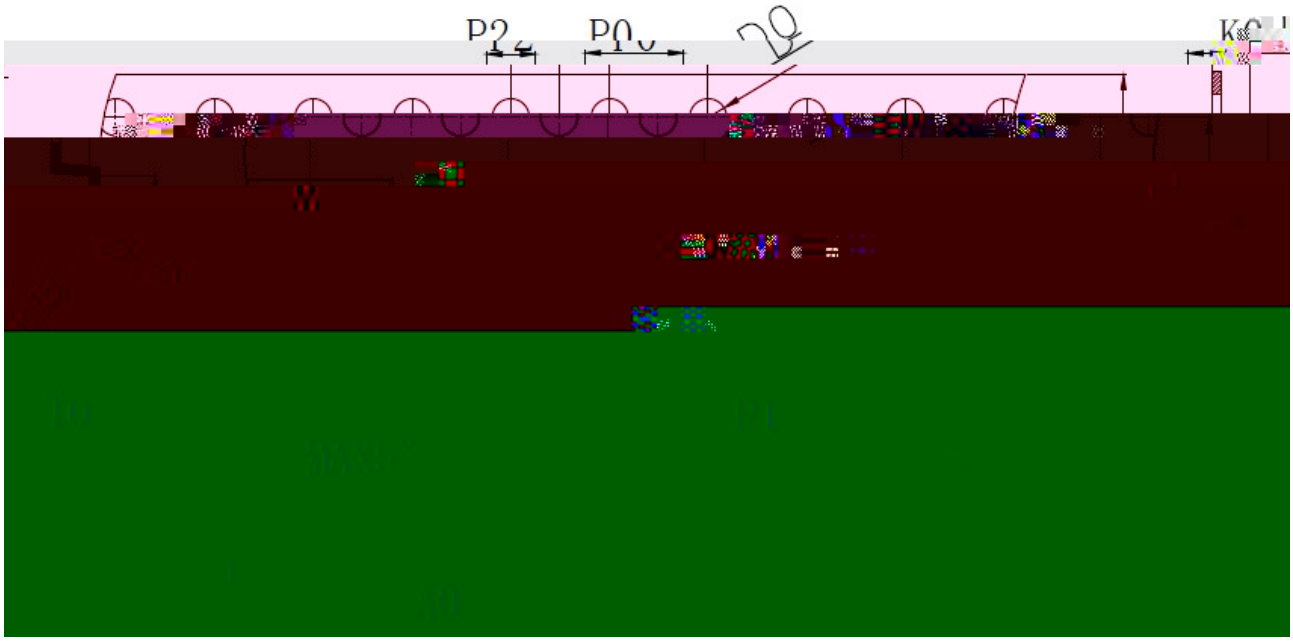
JST02G-800SWD

Order code	Voltage V_{DRM}/V_{RRM} (V)	IGT(mA)	Package	Base qty. (pcs)	Delivery mode
		- -			
JST02G-800SWD-TR	800	10	DFN5*6-8L	5,000	Tape & Reel

Document Revision History

Date	Revision	Changes
Oct.25, 2023	A.1.0	Last updated





SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	SYMBOL	[illegible]
75±0.10	5.50±0.10	1.55±0.05	1.55±0.10	12.00 +0.3 −0.1	SPEC	0.25±0.03	1.

PACKAGE	OUTLINE	REEL (PCS)	PER CARTON (PCS)	TAPE & REEL
DFN5*6-8L	TAPING	5,000	50,000	13 inch

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