

Average gate power dissipation ($T_j=150$)	$P_{G(AV)}$	1	W
Peak gate power	P_{GM}	10	W
Peak pulse voltage ($T_j=25$; non-repetitive, off-state; FIG.7)	V_{pp}	4	kV

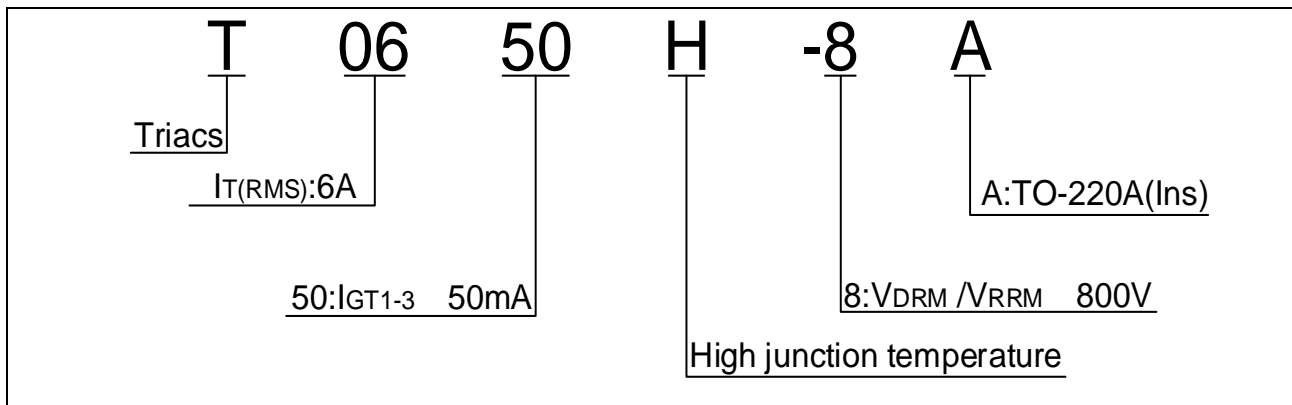
ELECTRICAL CHARACTERISTICS ($T_j=25$ unless otherwise specified)

Symbol	Test Condition	Qada	Value		Unit
I_{GT}	$V_D=12V R_L=33$	- -	MAX.	50	mA
V_{GT}		- -	MAX.	1	V
V_{GD}	$V_D=V_{DRM} T_j=150$ $R_L=3.3k$	- -	MIN.	0.2	V
I_L	$I_G=1.2I_{GT}$	-	MAX.	70	mA
				100	
I_H	$I_T=100mA$		MAX.	50	mA
dV/dt	$V_D=540V$ Gate Open $T_j=150$		MIN.	1200	V/s
$(dI/dt)_c$	$V_D=540V$ $T_j=150$		MIN.	5	A/ms
t_{on}	$I_G=80mA I_A=400mA I_R=40mA$ $T_j=25$		TYP.	5	s
t_{off}				50	

STATIC CHARACTERISTICS

Symbol	Parameter		Value (MAX.)	Unit
V_{TM}	$I_{TM}=8.5A t_p=380$ s	$T_j=25$	1.4	V
V_{TO}	Threshold voltage	$T_j=150$	0.8	V
R_D	Dynamic resistance	$T_j=150$	63	Ω
I_{DRM}	$V_D=V_{DRM} V_R=V_{RRM}$	$T_j=25$	5	A
I_{RRM}		$T_j=150$	1	mA

ORDERING INFORMATION



MARKING

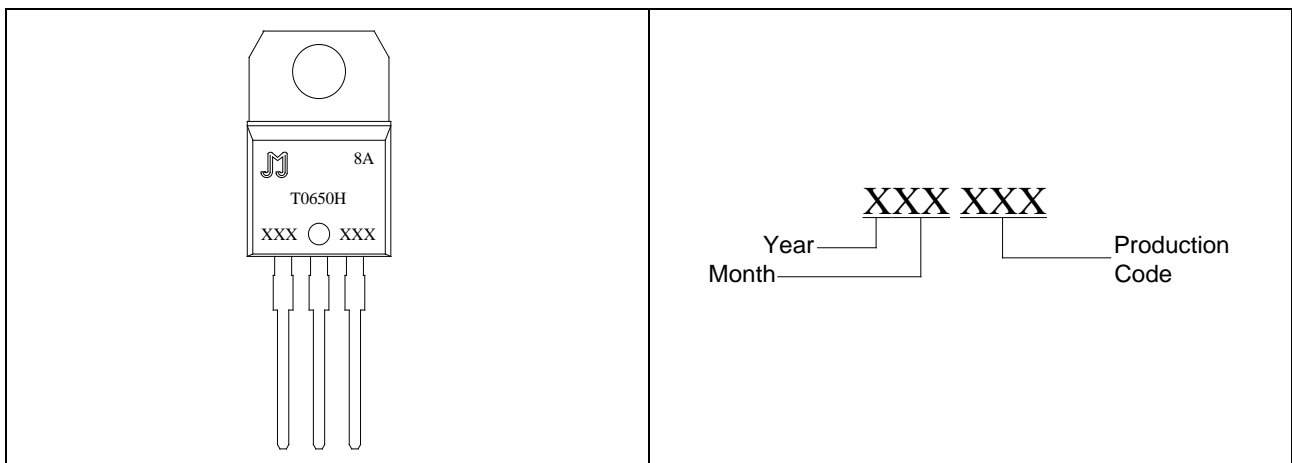


FIG.1: Maximum power dissipation versus RMS on-state current

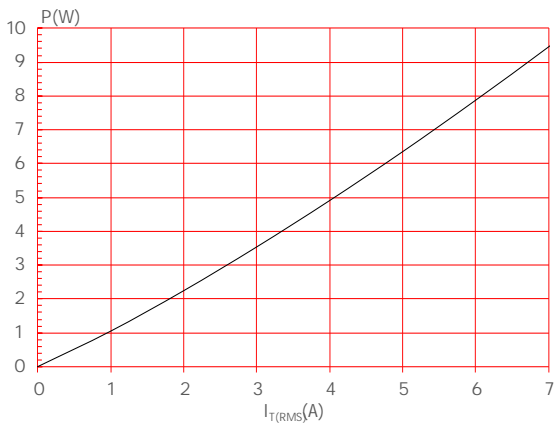
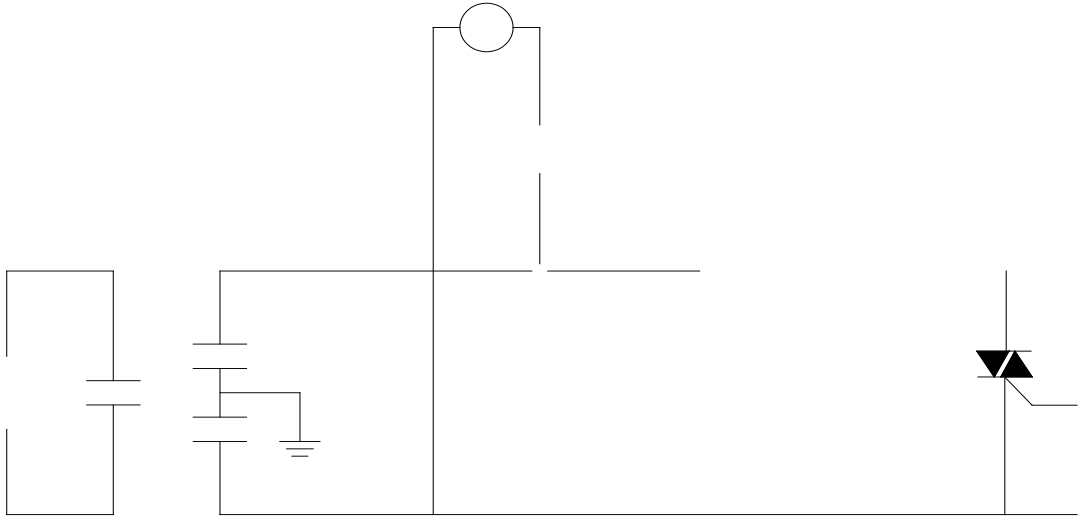


FIG.2: RMS on-state current versus case temperature



FIG.7 Test circuit for inductive and resistive loads to IEC-61000-4-5 standards




ORDERING INFORMATION

Order code	Voltage V_{DRM}/V_{RRM} (V)	IGT(A _m) H	Package	Base pin (pins)	Delivery date
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