

## Description

### JMT N-channel Enhancement Mode Power MOSFET

#### Features

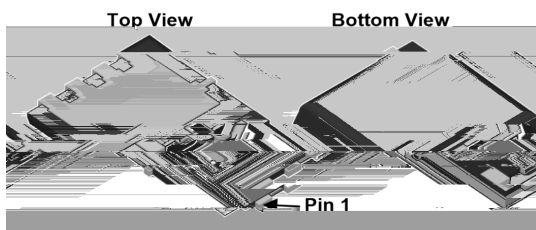
- 40V, 50A
- $R_{DS(ON)} < 6.6m\Omega @ V_{GS} = 10V$
- $R_{DS(ON)} < 9.4m\Omega @ V_{GS} = 4.5V$
- Advanced Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free

#### Applications

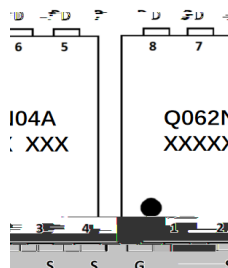
- Load Switch
- PWM Application
- Power Management



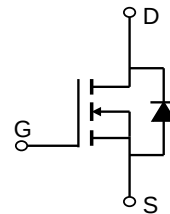
100% UIS TESTED!  
100%  $\hat{V}_{ds}$  TESTED!



PDFN3x3-8L



Marking and Pin Assignment



Schematic Diagram

## Package Marking and Ordering Information

| Device Marking | Device      | Outline | Package    | Reel Size | Reel(pcs) | Per Carton (pcs) |
|----------------|-------------|---------|------------|-----------|-----------|------------------|
| Q062N04A       | JMTQ062N04A | TAPING  | PDFN3x3-8L | 13"       | 5000      | 50000            |

## Absolute Maximum Ratings (@ $T_C = 25^\circ C$ unless otherwise specified)

| Symbol   | Parameter                                              | Value    | Units |
|----------|--------------------------------------------------------|----------|-------|
| $V_{DS}$ | Drain-to-Source Voltage                                | 40       | V     |
| $V_{GS}$ | Gate-to-Source Voltage                                 | $\pm 20$ | V     |
|          | $T$                                                    | 50       |       |
|          |                                                        | 32       |       |
|          | Pulsed Drain Current <sup>(1)</sup>                    | 200      |       |
|          | Single Pulsed Avalanche Energy <sup>(2)</sup>          | 100      |       |
|          | Power Dissipation                                      | 39       |       |
|          | Thermal Resistance, Junction to Ambient <sup>(3)</sup> | 43       |       |
|          | Thermal Resistance, Junction to Case                   | 3.2      |       |

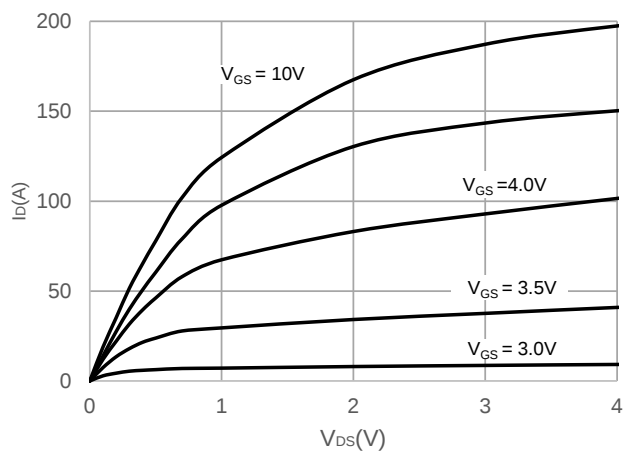
# Electrical Characteristics (T<sub>J</sub> = 25°C unless otherwise specified)

| Symbol               | Conditions | Min. | Typ. | Max. | Unit |
|----------------------|------------|------|------|------|------|
| Off Characteristics  |            |      |      |      |      |
| V <sub>(BR)DSS</sub> |            | 40   | -    | -    | V    |
| I <sub>DSS</sub>     |            | -    | -    | 1.0  | A    |
| I <sub>GSS</sub>     |            | -    | -    | ±100 | nA   |
|                      |            |      |      |      |      |
| V <sub>GS(th)</sub>  |            | 1.3  | 1.8  | 2.3  | V    |
|                      |            | -    | 5.1  | 6.6  | m    |
|                      |            | -    | 7.2  | 9.4  | m    |
|                      |            |      |      |      |      |
| C <sub>iss</sub>     |            | -    | 3031 | -    | pF   |
| C <sub>oss</sub>     |            | -    | 213  | -    | pF   |
| C <sub>rss</sub>     |            | -    | 179  | -    | pF   |
| Q <sub>g</sub>       |            | -    | 59   | -    | nC   |
| Q <sub>gs</sub>      |            | -    | 12   | -    | nC   |
| Q <sub>gd</sub>      |            | -    | 12   | -    | nC   |
|                      |            |      |      |      |      |
| t <sub>d(on)</sub>   |            | -    | 11   | -    | ns   |
| t <sub>r</sub>       |            | -    | 32   | -    | ns   |
| t <sub>d(off)</sub>  |            | -    | 52   | -    | ns   |
| t <sub>f</sub>       |            | -    | 13   | -    | ns   |
|                      |            |      |      |      |      |
| I <sub>S</sub>       |            | -    | -    | 50   | A    |
| I <sub>SM</sub>      |            | -    | -    | 200  | A    |
| V <sub>SD</sub>      |            | -    | -    | 1.2  | V    |
| trr                  |            | -    | 13   | -    | ns   |
| Qrr                  |            | -    | 7    | -    | nC   |

Notes

## Typical Performance Characteristics

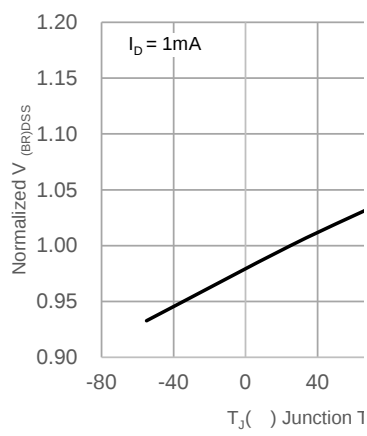
Figure 1: Output Characteristics





## Typical Performance C

Figure 7: Normalized Bi  
Junction Te



## Test Circuit

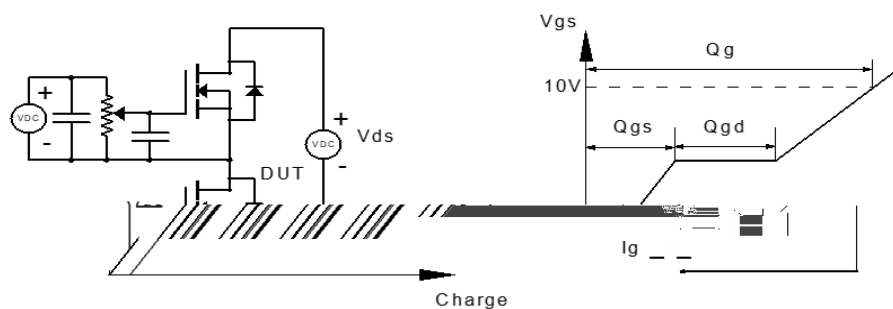


Figure 1: Gate Charge Test Circuit & Waveform

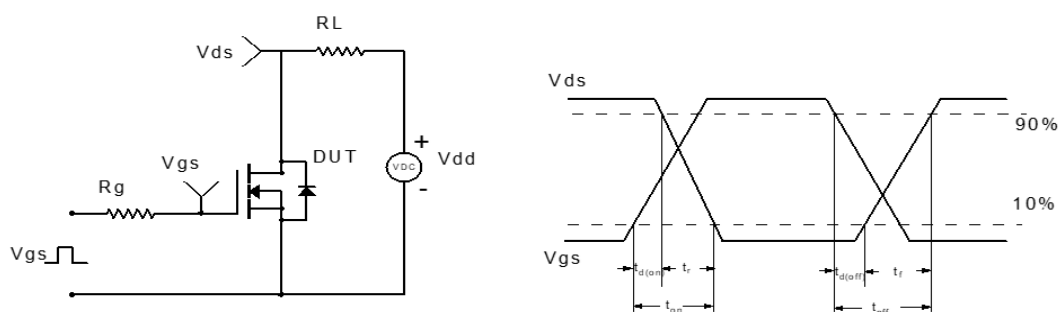


Figure 2: Resistive Switching Test Circuit & Waveform

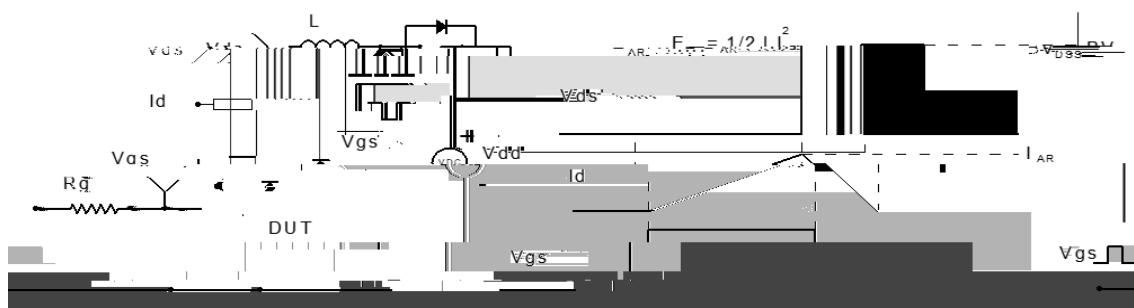


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

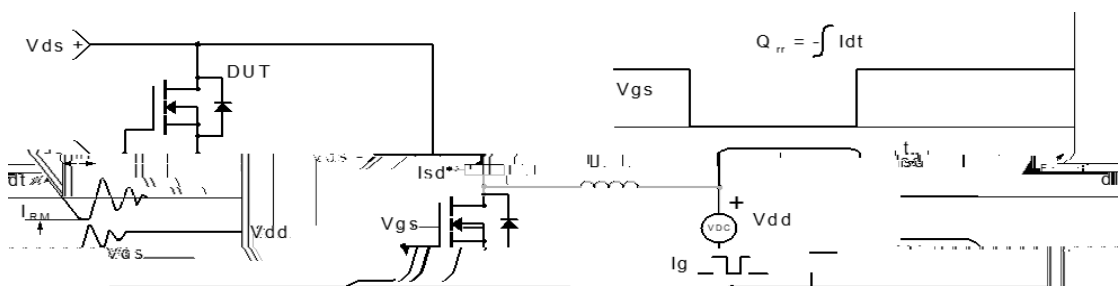


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(PDFN3x3-8L)